REMARKS

The following remarks are fully and completely responsive to the Office Action dated April 16, 2003. Claims 1-11 and 19-37 are pending in this application with claims 30-37 added by the present Amendment and claims 12-18 withdrawn. In the outstanding Office Action, claims 1-11 and 19-29 were rejected under 35 U.S.C. § 102(e). No new matter has been entered. Claims 1-11 and 19-37 are presented for consideration.

35 U.S.C. § 102(e)

Claims 1-11 and 19-29 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wert (U.S. Patent No. 6,281,706). In making this rejection, the Office Action asserts that this reference teaches each and every element of the claimed invention. Applicants respectfully request reconsideration of this rejection.

Claim 1 recites a method of controlling an output buffer circuit for generating an output signal and outputting the output signal from an output terminal. The output buffer circuit includes a first drive circuit for receiving an input signal and a second drive circuit connected to the output terminal. The method includes generating a first output signal having a first state in accordance with the input signal using the first drive circuit. The first state indicates one of a high logical level and a low logical level. The second drive circuit is driven to generate a second output signal having the first state by a driving signal which is generated by adding a predetermined delay to the output signal.

Claim 5 recites an output buffer circuit. This circuit includes a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first

output signal having a first state indicative of one of a high logical level and a low logical level. A second drive circuit is connected to the output terminal. The second drive circuit generates a second output signal. A first control circuit is connected to the second drive circuit for generating a first control signal for driving the second drive circuit on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the first state.

Accordingly, the second output circuit of the present invention is driven/controlled to generate a signal having a level that is the same as the first drive circuit output signal after receiving a driving/delay signal. The driving/delay signal is generated by adding a predetermined delay to the output signal.

Wert is directed to a boost circuit including a first drive circuit 701, 711, a second drive circuit 705, 717, and two inverters 707, 709. The second drive circuit 705, 717 of Wert is formed from two transistors – a PMOS transistor 705 and a NMOS transistor 717. The PMOS transistor 705 is driven when the boost enable signal BH_EN 303 is active; the control signal at terminal 311 is a low logic level (input to NAND 707 is a high logic level); and output 305 is a low logic level or between a low logic level and approximately 800 mV of the supply voltage V_{DD}. When the output 305 is within approximately 800 mV of supply voltage V_{DD}, the output of inverter 728 changes from a high logic level to a low logic level and turns off PMOS transistor 705. Thus, when PMOS transistor 705 receives the signal generated by adding a predetermined delay to the output signal, the PMOS transistor 705 turns off. Therefore, PMOS transistor 705 cannot generate a second output signal having the first state (the state of the output signal produced by the first drive circuit).

In contrast, the second drive circuit of the present invention is controlled to generate a signal having a level that is the same as that of the first drive circuit output signal. The difference between Wert and the present invention is based on Wert using the second drive circuit to quickly raise the output signal of the booster. In contrast, the present invention uses the first and second drive circuits to generate an output signal having a gentle wave form.

Accordingly, Wert fails to teach and/or suggest the recited invention. Specifically, Wert fails to teach and/or suggest driving the second drive circuit to generate a second output signal having the first state by a driving signal which is generated by adding a predetermined delay to the output signal. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-11 and 19-29 under 35 U.S.C. § 102(e).

New Claims

New claims 30 and 37 are added by the present Amendment to claim additional features of the present invention. For at least the reasons discussed above regarding claims 1-11 and 19-29, claims 30-37 are allowable. Accordingly, Applicants respectfully request consideration and allowance of claims 30-37.

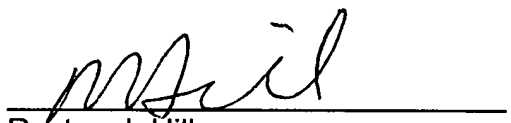
Conclusion

Applicants' remarks have overcome the rejection set forth in the Office Action dated April 16, 2003. Specifically, Applicants' remarks have distinguished claims 1-11 and 19-29 from Wert, and thus overcome the rejection of these claims under 35 U.S.C. § 102(e). New claims 30 and 37 have been added to further claim Applicants' invention. Accordingly, claims 1-11 and 19-37 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-11 and 19-37.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 108075-00022.

Respectfully submitted,



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Enclosure: Petition for Extension of Time